REMARKS

The claims are claims 1 to 20.

The application has been amended at many locations to correct minor errors and to present uniform language throughout. These amendments include a SUMMARY OF THE INVENTION.

Claims 1 to 5, 9 to 14 and 16 to 18 are amended. Claims 1 to 5, 9 to 14 and 16 to 18 were amended to make clear that the first and second groups of bits are of the parameter value.

A TERMINAL DISCLAIMER relative to U. S. Patent No. 6,912,675 is attached. This TERMINAL DISCLAIMER obviates the double patenting rejection of claims 1 to 20.

Claims 1 to 17 were rejected under 35 U.S.C. 102(e) as being anticipated by Edwards U.S. Patent Application No. 6,779,145.

Claims 1 and 11 recite subject matter not anticipated by Edwards. Claims 1 and 11 recite "detecting a condition wherein the bits of a first group within the plurality of bits of said parameter value all have the same bit value and a predetermined bit within a second group of the plurality of bits of said parameter value has a bit value equal to the bit value of the bits of first group." The OFFICE ACTION cites Edwards at column 12, lines 4 to 16 as anticipating this subject matter. This portion of Edwards states:

> "As discussed above, trace information may include state information of processor 102. For example, a watchpoint channel may be defined in processor 102 that "watches" for a particular state condition in processor 102 and triggers an event signal to debug circuit 103 when the condition occurs. A watchpoint channel may include a mechanism by which a data value associated with an execution pipeline in processor 102 may be matched to one or more predetermined data values. For example, predetermined data values stored in registers associated with processor 102 may be compared with data values in processor 102 including instruction addresses, instruction

value addresses, operand addresses, performance counters, event counters, and the like."

This portion of Edwards teaches triggering an event signal to debug circuit 103 when data values in processor 102 such as "instruction addresses, instruction value addresses, operand addresses, performance counters, event counters, and the like" matches one or more predetermined values. This portion of Edwards makes clear that the data values in processor 102 and the predetermined values are independent. In contrast, claims 1 and 11 recite detecting a condition in which a first group of bits all have the same value and match a predetermined bit of a second group of bits. As amended, claims 1 and 11 make clear that the first and second group of bits are both part of the recited parameter value. Edwards fails to disclose detecting when plural bits are all the same nor when these same bits match a predetermined bit of a second part of the same parameter value. Accordingly, claims 1 and 11 are allowable over Edwards.

Claims 1 and 11 recite further subject matter not anticipated by Edwards. Claims 1 and 11 recite outputting "only the second group of bits of said parameter value without outputting the first group of bits of said parameter value." The OFFICE ACTION cites column 12, lines 17 to 26 of Edwards as anticipating this subject matter. This portion of Edwards states:

> "When matched, a controller associated with the watchpoint channel may provide an event signal to debug circuit 103 through communication link 104. The signal may take the form of state bits indicating particular watchpoint channel states within processor 102. Also, state bit values corresponding to watchpoint channels may be combined together to produce other state bit values to be used in different debugging operations by debug circuit 103, and these other state bit values may also be communicated to debug circuit 103."

This portion of Edwards teaches outputting an event signal the may take the form of "state bits indicating particular watchpoint channel states." This portion of Edwards fails to teach that these state bits are the same as the second group of bits of the parameter value as recited in claims 1 and 11. Accordingly, claims 1 and 11 are allowable over Edwards.

Claim 2 recites subject matter not anticipated by Edwards. Claim 2 recites "receiving only the second group of bits of said parameter value externally of the data processor, and recreating the first group of bits of said parameter value based on the bit value of said predetermined bit." The OFFICE ACTION cites response message 509 and request message 501 illustrated in Figure 5 of Edwards as anticipating this subject matter. Edwards states at column 11, lines 25 to 36:

> "FIG. 5 shows request 501, response 509, and trace 517 messages that may be transmitted by a debug circuit 103 to external system 106. Request message 501 may include a message type field 502, request opcode 503, address 504, source 505, TID 506, mask 507, and data 508 fields which are similar in format and function to similarly-named fields of request message 401. Further, debug circuit 103 may be configured to send a response message 509 to an external system 106, response message 509 including message type 510, response opcode 511, dummy 512, source 513, TID 514, dummy 515, and data 516 fields similar in form and function to similarly-named fields of response message 408."

This is the only mention of elements 501 and 509 in Edwards. The first sentence of this portion of Edwards makes clear that both the request message 501 and the response message 509 are transmitted by debug circuit 103 to external system 106. Accordingly, neither request message 501 nor response message 509 can be the result of "recreating of the first group of bits" as recited in claim 2. Edwards fails to state that either request message 501 or response message 509 is the second group of bits supposedly taught in

Edwards at column 12, lines 4 to 26 as recited in claim 2. Accordingly, claim 2 is allowable over Edwards.

Claims 3 and 12 recite subject matter not anticipated by Edwards. Claims 3 and 12 recite "the first group of bits of said parameter value includes at least one byte, the second group of bits of said parameter value includes at least one byte, and the predetermined bit is a most significant bit of said at least one byte of the second group of bits of said parameter value." The OFFICE ACTION cites column 24, lines 58 to 60 of Edwards as anticipating this subject matter. Edwards states at column 24, lines 58 to 61:

> "(3) External system 106 can send status information and from 1-byte to 4-bytes of an input message to JTAG debug register 1201 (13, 21, 29, or 37-bits of JTAG debug register 1201 are shifted)."

This disclosure of Edwards teaches a 1-byte to 4-byte status information message. This passage of Edwards teaches neither that the first group of bits of the parameter value is at least one byte, that the second group of bits of the parameter value is at least one byte nor which bit within the second group of bits of the parameter value is the predetermined bit. The Applicants submit that Edwards must at least mention the recited "predetermined bit" and the "most significant bit" to anticipate that the most significant bit is the predetermined bit. Accordingly, claims 3 and 12 are allowable over Edwards.

Claims 4 and 13 recite subject matter not anticipated by Edwards. Claims 4 and 13 recite "the second group of bits of said parameter value includes a plurality of bytes and the predetermined bit is a most significant bit of one of the bytes of the second group of bits of said parameter value." The OFFICE ACTION cites column 24, lines 58 to 60 of Edwards as anticipating this subject

matter. This portion of Edwards is quoted above. This disclosure of Edwards teaches a 1-byte to 4-byte status information message. This passage of Edwards teaches neither that the second group of bits of the parameter value includes a plurality of bytes nor which bit within the second group of bits of the parameter value is the predetermined bit. The Applicants submit that Edwards must at least mention the recited "predetermined bit" and the "most significant bit" to anticipate that the most significant bit of one byte is the predetermined bit. Accordingly, claims 4 and 13 are allowable over Edwards.

Claims 5 and 14 recite subject matter not anticipated by Edwards. Claims 5 and 14 recite the "one byte of the second group of bits of said parameter value is a most significant byte of the second group of bits of said parameter value." Respective base claims 4 and 13 recite that this "one byte" is the byte containing the predetermined bit. The OFFICE ACTION cites column 24, lines 58 to 60 of Edwards as anticipating this subject matter. This portion of Edwards is quoted above. This disclosure of Edwards teaches a 1-byte to 4-byte status information message. This passage of Edwards fails to teach that byte of the second group of bits of the parameter value including the predetermined bit is the most significant byte of the second group of bits of the parameter value is. The Applicants submit that Edwards must at least mention the recited "one byte of the second group of bits" and the "most significant byte" to anticipate that the one byte is the most significant byte. Accordingly, claims 5 and 14 are allowable over Edwards.

Claims 9, 10, 16 and 17 recite subject matter not anticipated by Edwards. Claims 9 and 16 recite that "said bit value of said predetermined bit and said bits of said first group of said parameter value is 1." Claims 10 and 18 recite that "said bit value of said predetermined bit and said bits of said first group

of said parameter value is 0." The OFFICE ACTION cites the PC Absolute entry in Table 1 appearing at column 13 of Edwards as anticipating this subject matter. This table entry states:

> "PC Absolute 1-bits [12] Defines whether a program counter (PC) field contains a 4-byte absolute address or a 1- or 2-byte relative address. A relative address is the signed offset from the most recent PC value sent in a previous trace message (of any type).
> "Value - Description
> "0 - Relative address offset
> "1 - Absolute 4-byte address"

The "0" or "1" in the PC Absolute field indicate whether the PC filed is a relative or absolute address. This PC Absolute field does not indicate either that the first group of bits and the predetermined bit of the second group of bits is "0" or that the first group of bits and the predetermined bit of the second group of bits is "1." The PC Absolute field does not signal that bits in the PC field are "0" or "1." Accordingly, claims 9, 10, 16 and 17 are allowable over Edwards.

Claims 18 to 20 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards U.S. Patent Application No. 6,779,145 and Asano U.S. Patent Application No. 5,572,710.

Claim 18 recites subject matter not made obvious by the combination of Edwards and Asano. Claim 18 recites "an evaluator coupled to said input for detecting a condition wherein the bits of a first group within the plurality of bits of said parameter value all have the same bit value and a predetermined bit within a second group of the plurality of bits of said parameter value has a bit value equal to the bit value of the bits of said first group." The OFFICE ACTION cites column 12, lines 5 to 12 of Edwards as making obvious this limitation. This portion of Edwards is quoted above.

This portion of Edwards teaches triggering an event signal to debug circuit 103 when data values in processor 102 such as "instruction addresses, instruction value addresses, operand addresses, performance counters, event counters, and the like" matches one or more predetermined values. This portion of Edwards makes clear that the data values in processor 102 and the predetermined values are independent. In contrast, claim 18 recites detecting a condition in which a first group of bits all have the same value and match a predetermined bit of a second group of bits. As amended, claim 18 makes clear that the first and second group of bits are both part of the recited parameter value. Edwards fails to disclose detecting when plural bits are all the same nor when these same bits match a predetermined bit of a second part of the same parameter value. Accordingly, claim 18 is allowable over the combination of Edwards and Asano.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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